



# TVS Diodes

Transient Voltage Suppressor Diodes

## ESD102-U1-02ELS

Uni-directional Ultra-low Capacitance ESD / Transient Protection Diode

ESD102-U1-02ELS

## Data Sheet

Revision 1.0, 2013-02-04  
Final

Power Management & Multimarket

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**Revision History: Revision 0.9.1, 2012-07-27**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.0, 2013-02-04</b>	
All	Status change to Final

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Last Trademarks Update 2010-06-09

## 1 Uni-directional Ultra-low Capacitance ESD / Transient Protection Diode

### 1.1 Features

- ESD / Transient protection of high speed data lines exceeding
  - IEC61000-4-2 (ESD):  $\pm 20 \text{ kV}$  (air / contact)
  - IEC61000-4-4 (EFT):  $\pm 2.5 \text{ kV} / 50 \text{ A}$  (5/50 ns)
  - IEC61000-4-5 (surge):  $\pm 3 \text{ A}$  (8/20  $\mu\text{s}$ )
- Maximum working voltage:  $V_{RWM} = 3.3 \text{ V}$
- Ultra low capacitance  $C_L = 0.4 \text{ pF}$  (typical)
- Very low clamping voltage:  $V_{CL} = 8 \text{ V}$  (typical) at  $I_{PP} = 16 \text{ A}$  [2]
- Very low dynamic resistance:  $R_{DYN} = 0.19 \Omega$  (typical) [2]
- Pb-free (RoHS compliant) and halogen free package, very small form factor  $0.62 \times 0.32 \times 0.31 \text{ mm}^3$



### 1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

### 1.3 Product Description

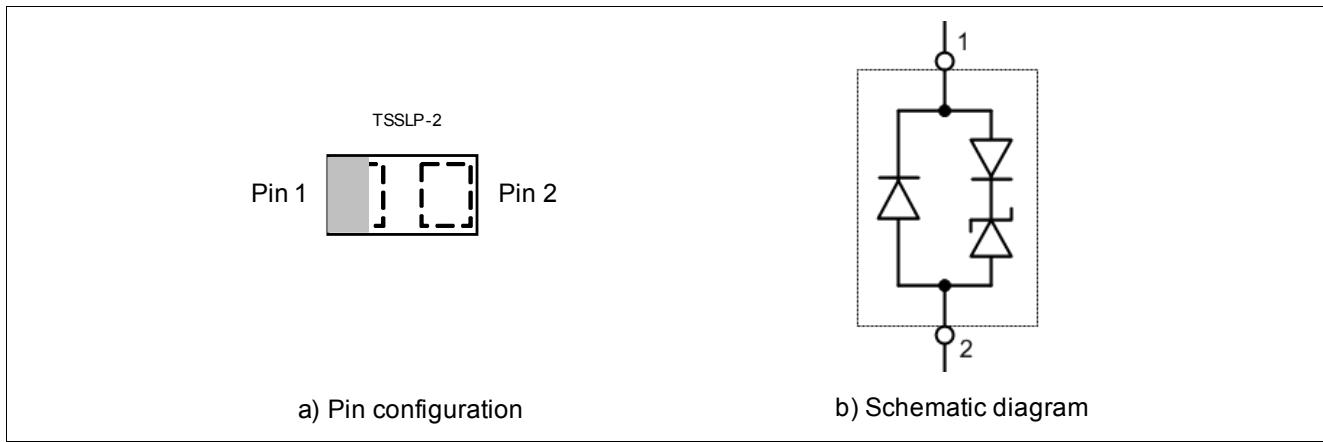


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD102-U1-02ELS	TSSLP-2-3	1 line, uni-directional	E

## 2 Characteristics

**Table 2 Maximum Rating at  $T_A = 25^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge <sup>1)</sup>	$V_{\text{ESD}}$	-20	—	20	kV
Peak pulse current ( $t_p = 8/20 \mu\text{s}$ ) <sup>2)</sup>	$I_{\text{PP}}$	-3	—	3	A
Operating temperature range	$T_{\text{OP}}$	-40	—	125	°C
Storage temperature	$T_{\text{stg}}$	-65	—	150	°C

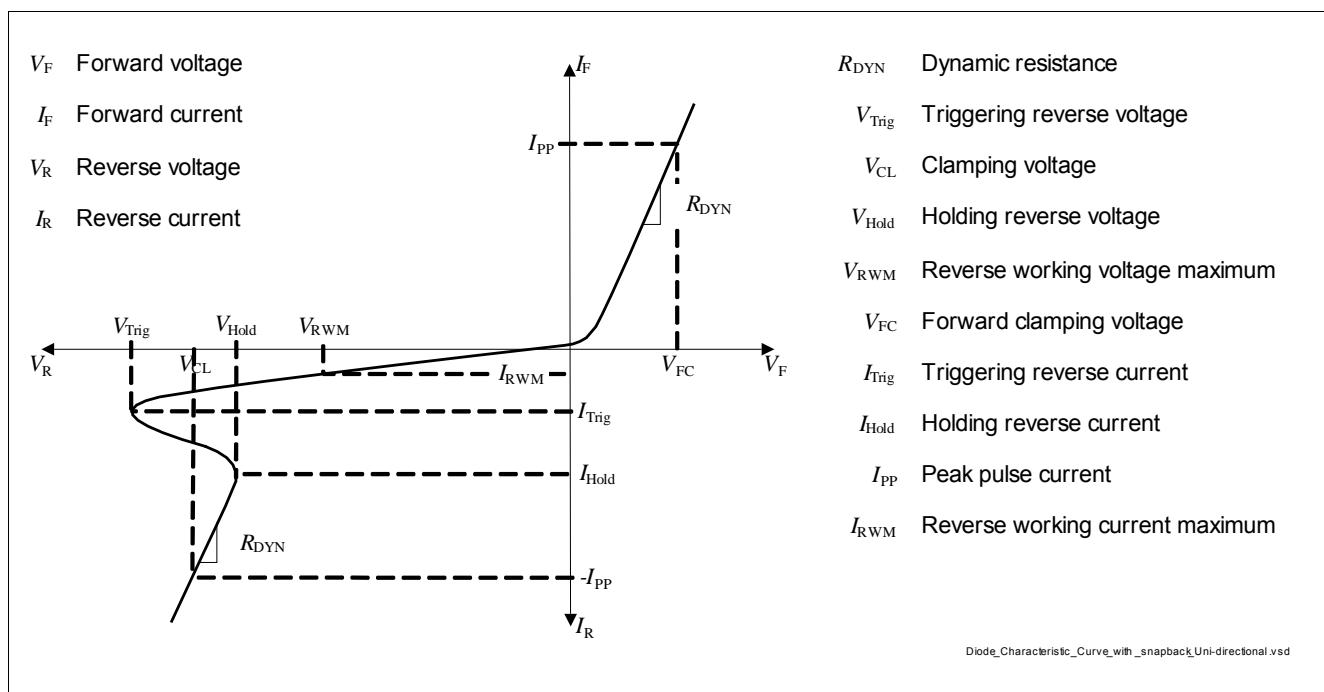
1)  $V_{\text{ESD}}$  according to IEC61000-4-2 ( $R = 330 \Omega$ ,  $C = 150 \text{ pF}$ )

2)  $I_{\text{PP}}$  according to IEC61000-4-5

**Attention: Stresses above the max. values listed here may cause permanent damage to the device.**

**Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

### 2.1 Electrical Characteristics at $T_A = 25^\circ\text{C}$ , unless otherwise specified



**Figure 2 Definitions of Electrical Characteristics**

## Characteristics

**Table 3 DC Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	—	—	3.3	V	Pin 1 to Pin 2
Breakdown voltage	$V_{BR}$	—	6.5	—	V	from Pin 1 to Pin 2 voltage forced
Reverse current	$I_R$	—	1	50	nA	$V_R = 3.3 \text{ V}$ , from Pin 1 to Pin 2

**Table 4 RF Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance <sup>1)</sup>	$C_L$	—	0.4	0.65	pF	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$
		—	0.4	0.65	pF	$V_R = 0 \text{ V}, f = 1 \text{ GHz}$
Series inductance	$L_S$	—	0.2	—	nH	

1) Total capacitance line to ground

**Table 5 ESD Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trigger voltage <sup>1)</sup> [2]	$V_{TRIG}$	—	7.2	—	V	TLP, from Pin 1 to Pin 2
Reverse clamping voltage <sup>1)</sup> [2]	$V_{CL}$	—	8	—	V	TLP, $I_{PP} = 16 \text{ A}$ , from Pin 1 to Pin 2
		—	11	—	V	TLP, $I_{PP} = 30 \text{ A}$ , from Pin 1 to Pin 2
Forward clamping voltage <sup>1)</sup> [2]	$V_{FC}$	—	6	—	V	TLP, $I_{PP} = 16 \text{ A}$ , from Pin 2 to Pin 1
		—	9	—	V	TLP, $I_{PP} = 30 \text{ A}$ , from Pin 2 to Pin 1
Dynamic resistance <sup>1)</sup> [2]	$R_{DYN}$	—	0.19	—	$\Omega$	TLP, Pin 1 to Pin 2
		—	0.23	—	$\Omega$	TLP, Pin 2 to Pin 1

1) Please refer to Application Note AN210. ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP),  $t_p = 100\text{ns}$ ,  $t_r = 0.6 \text{ ns}$ ,  $I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ , extraction of dynamic TLP characteristic between  $I_{PP1} = 10 \text{ A}$  and  $I_{PP2} = 40 \text{ A}$ .

## 2.2 Typical Characteristics at $T_A=25^\circ\text{C}$ , unless otherwise specified

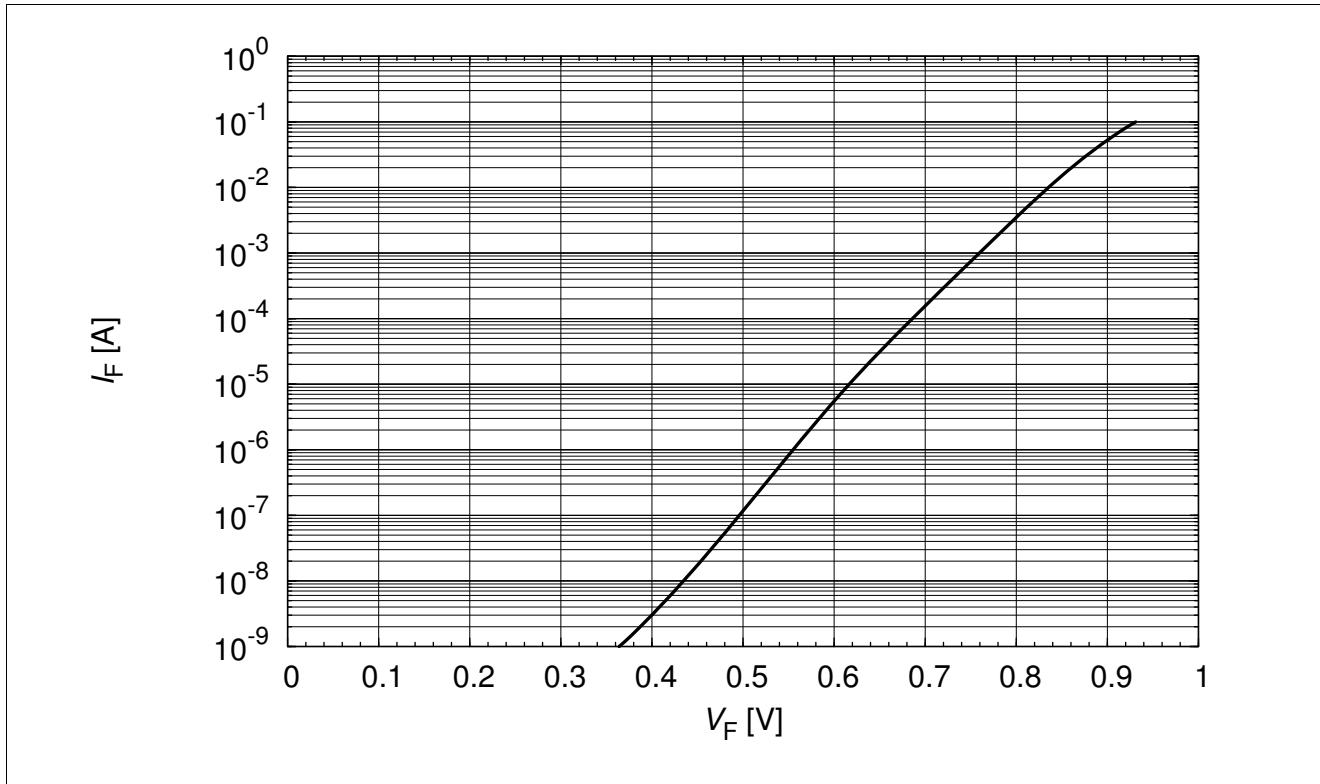


Figure 3 Forward current,  $I_F = (V_F)$

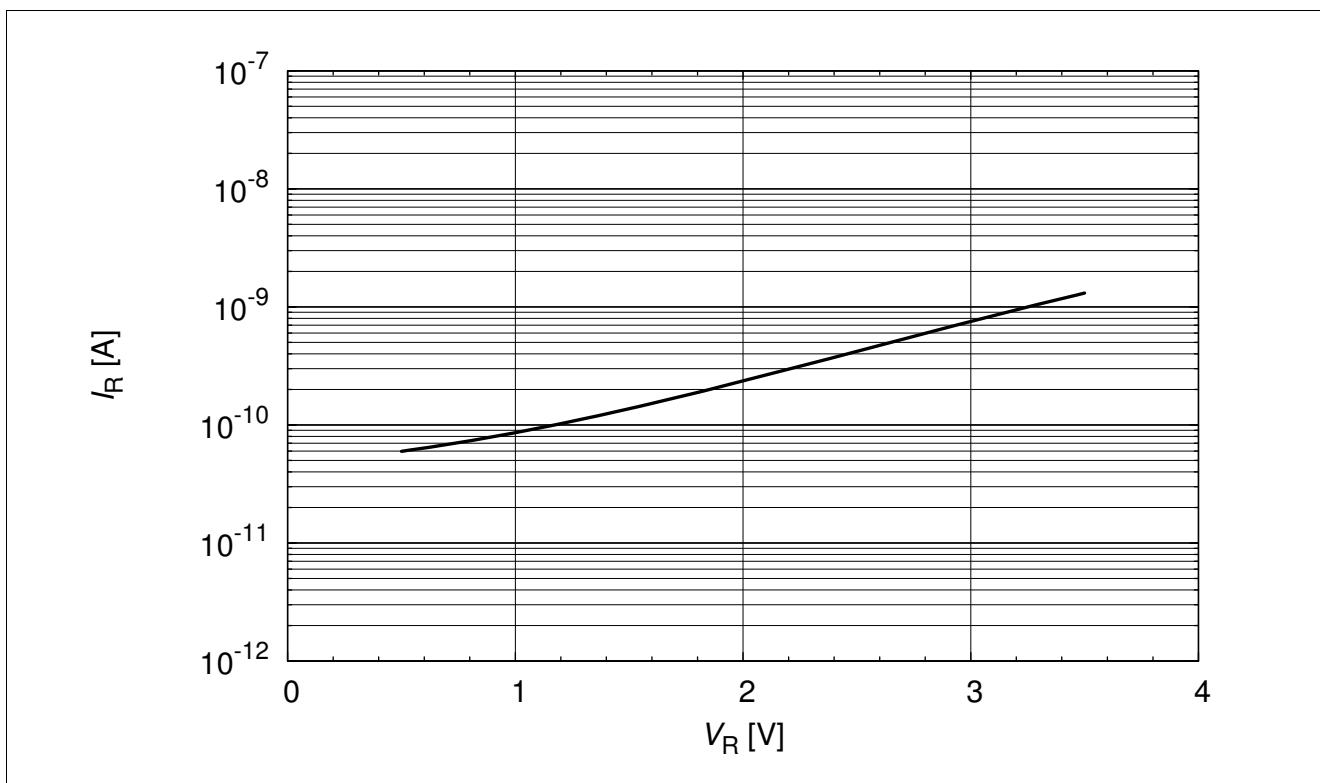
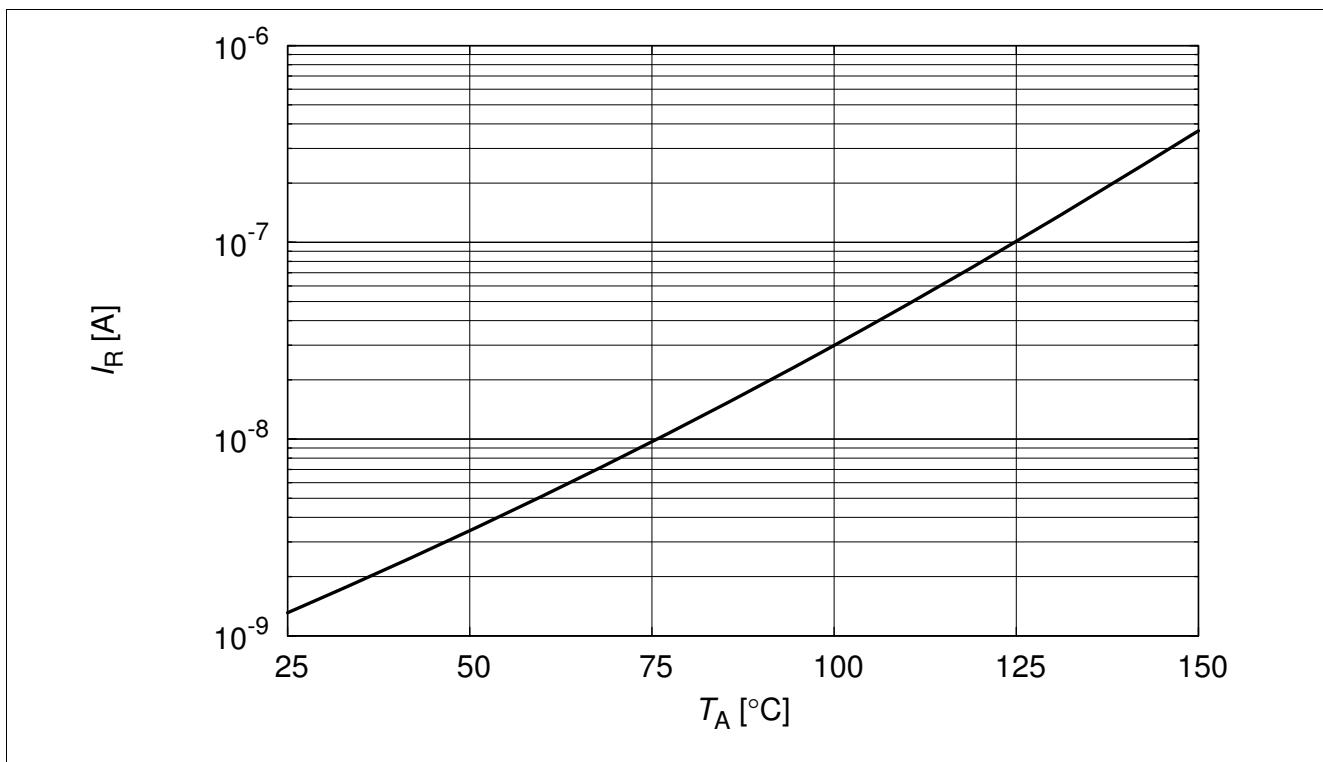
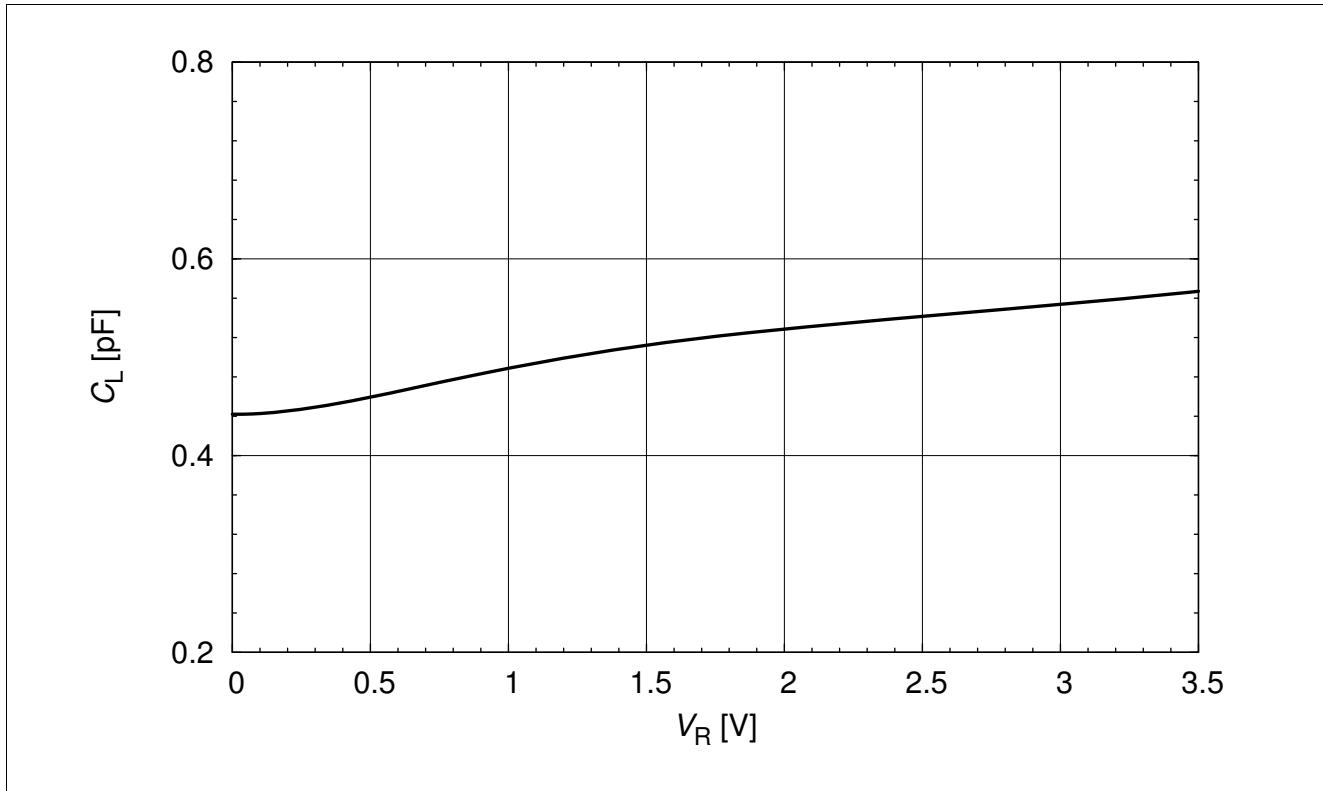


Figure 4 Reverse current,  $I_R = (V_R)$

**Characteristics**

**Figure 5** Reverse current  $I_R = f(T_A)$ ,  $V_R = 3.3$  V

**Figure 6** Line capacitance  $C_L = f(V_R)$ ,  $f = 1$  MHz, from pin 1 to pin 2

## Characteristics

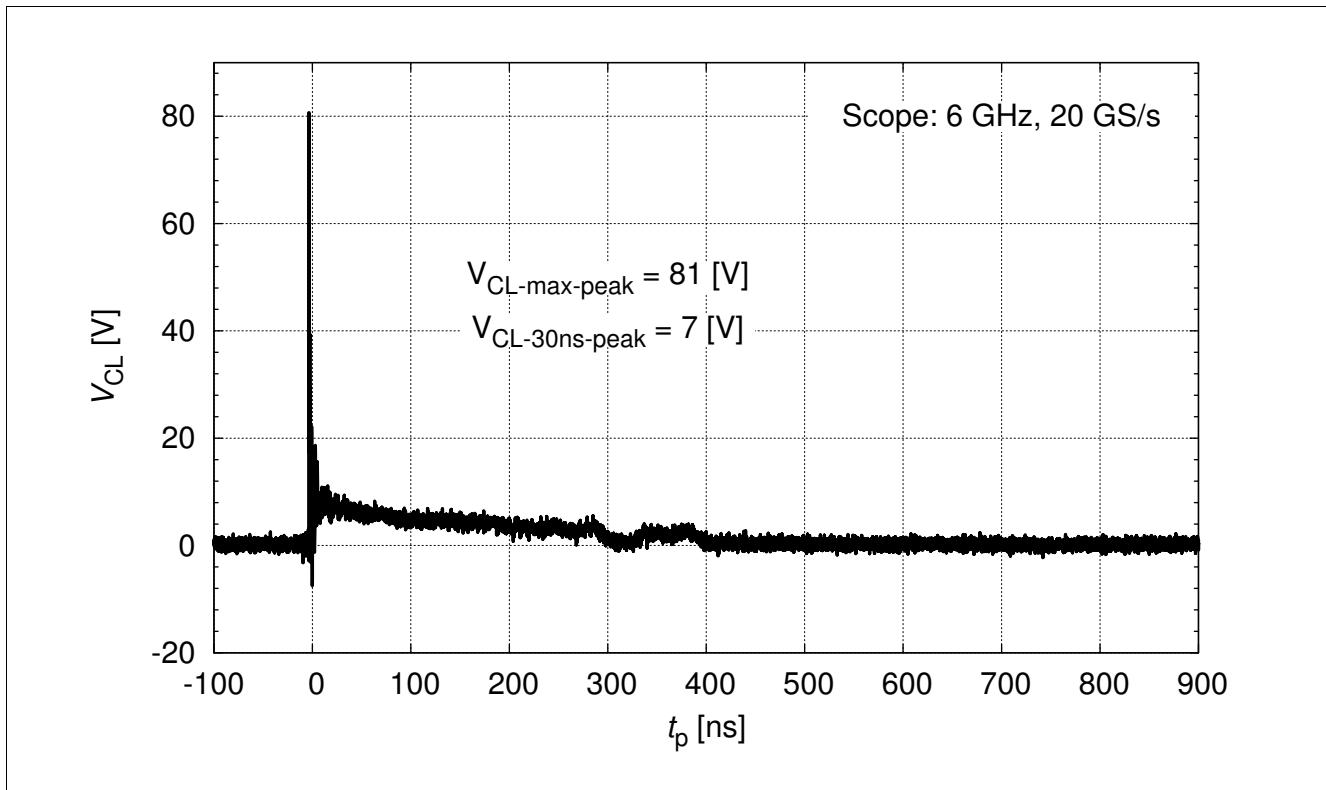


Figure 7 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV positive pulse from pin 1 to pin 2

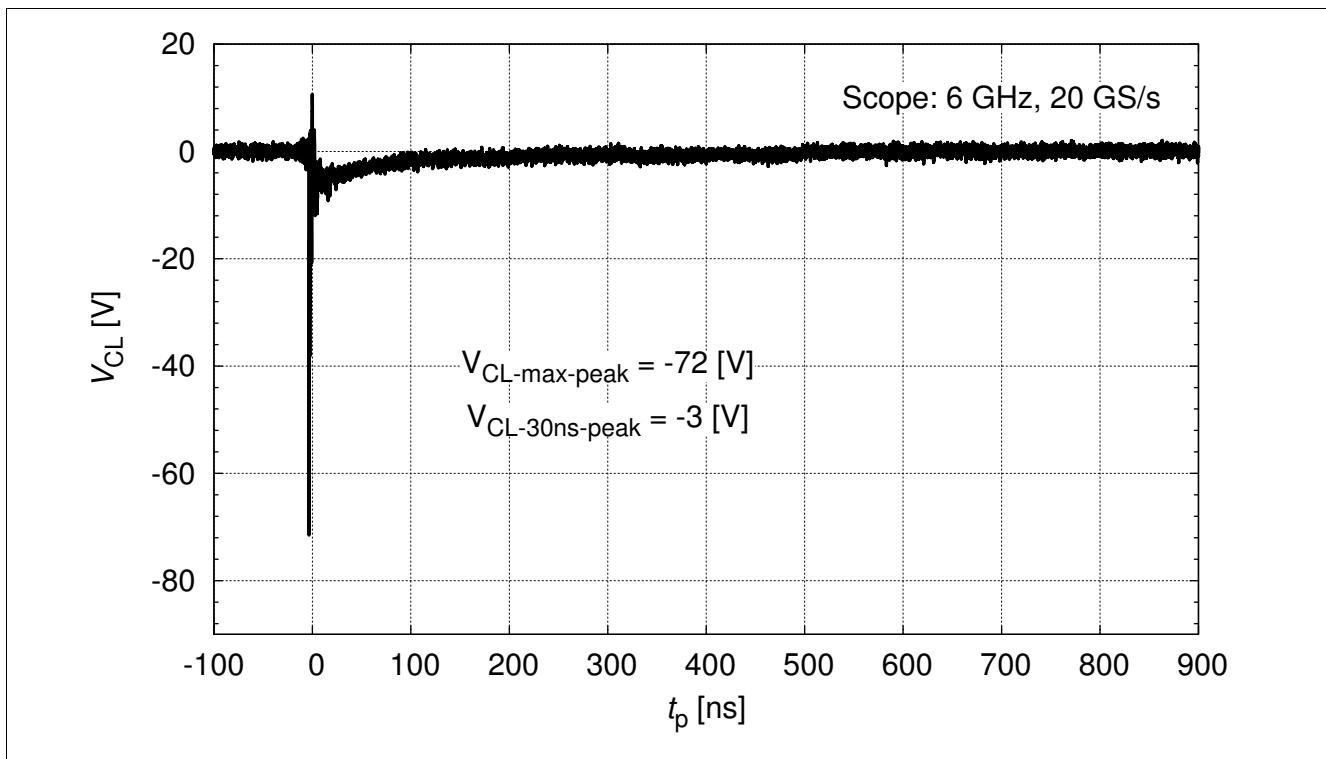
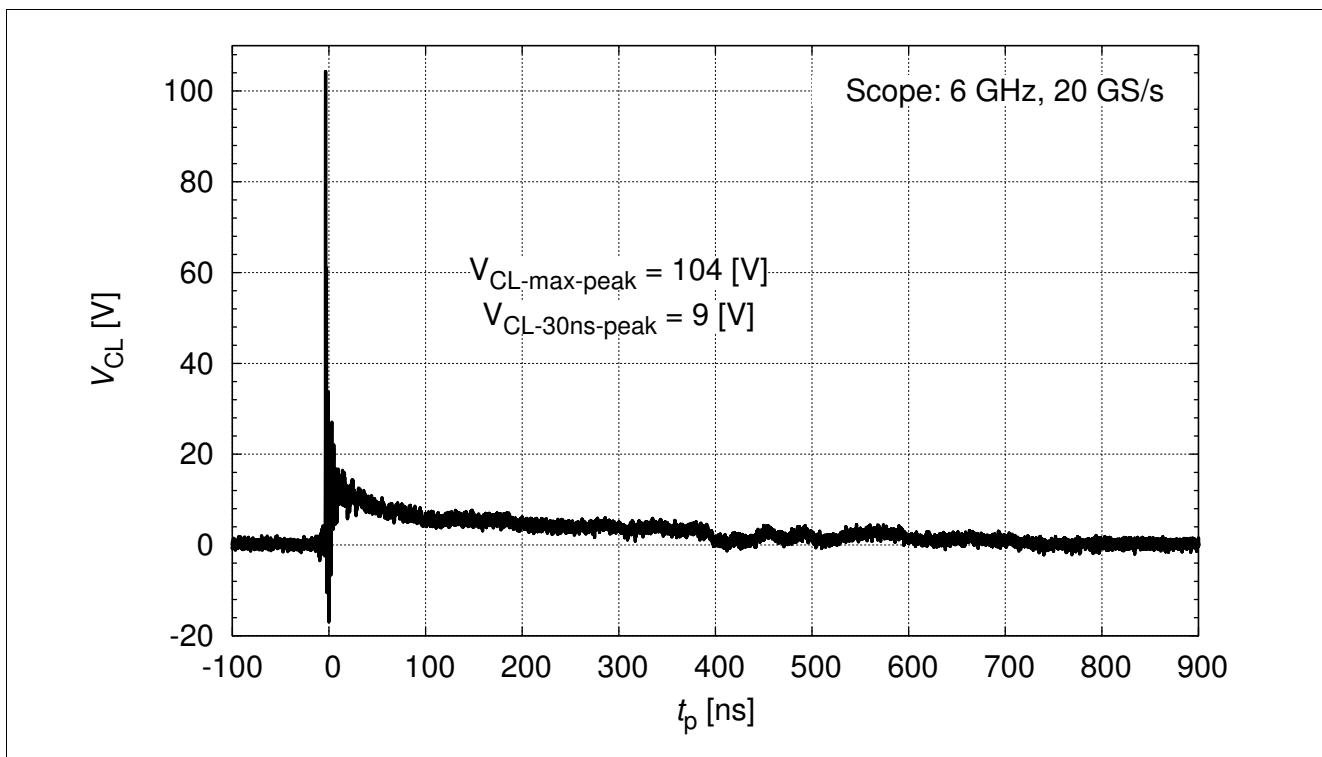
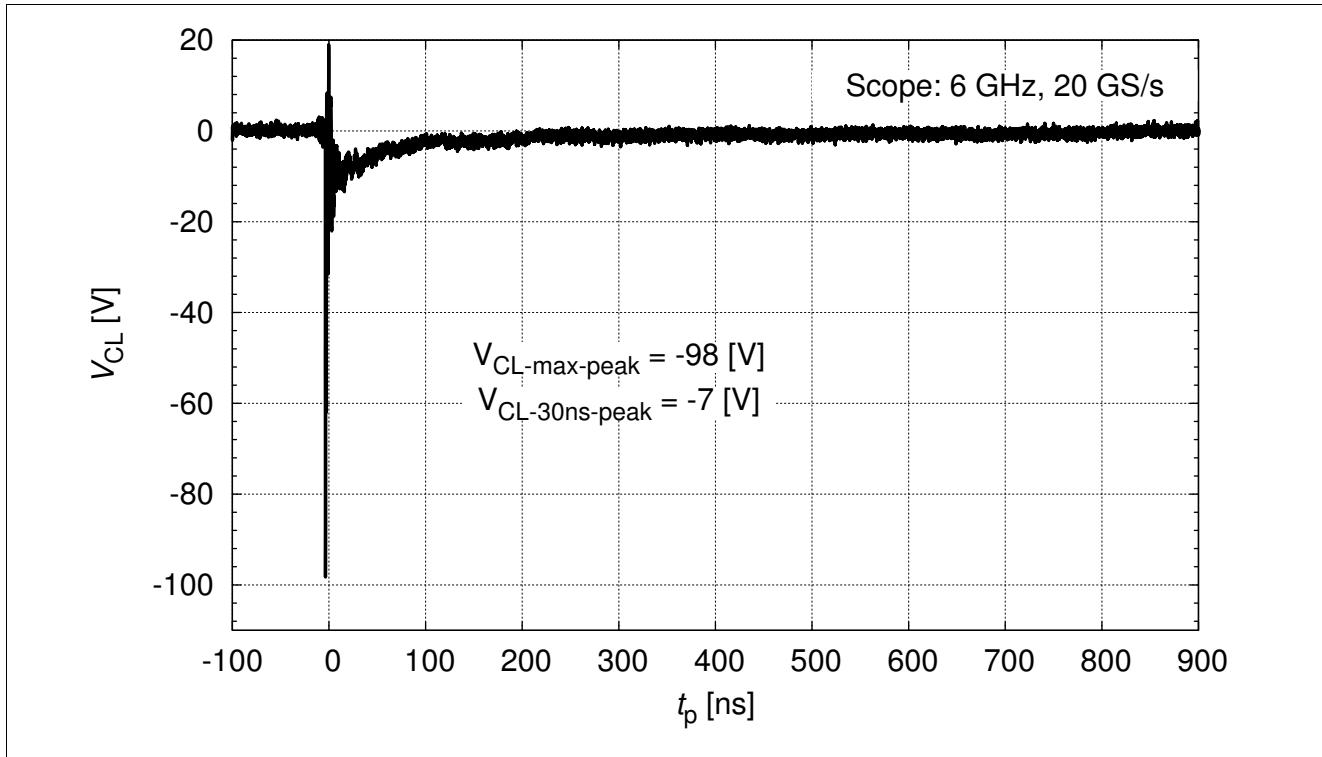


Figure 8 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV negative pulse from pin 1 to pin 2

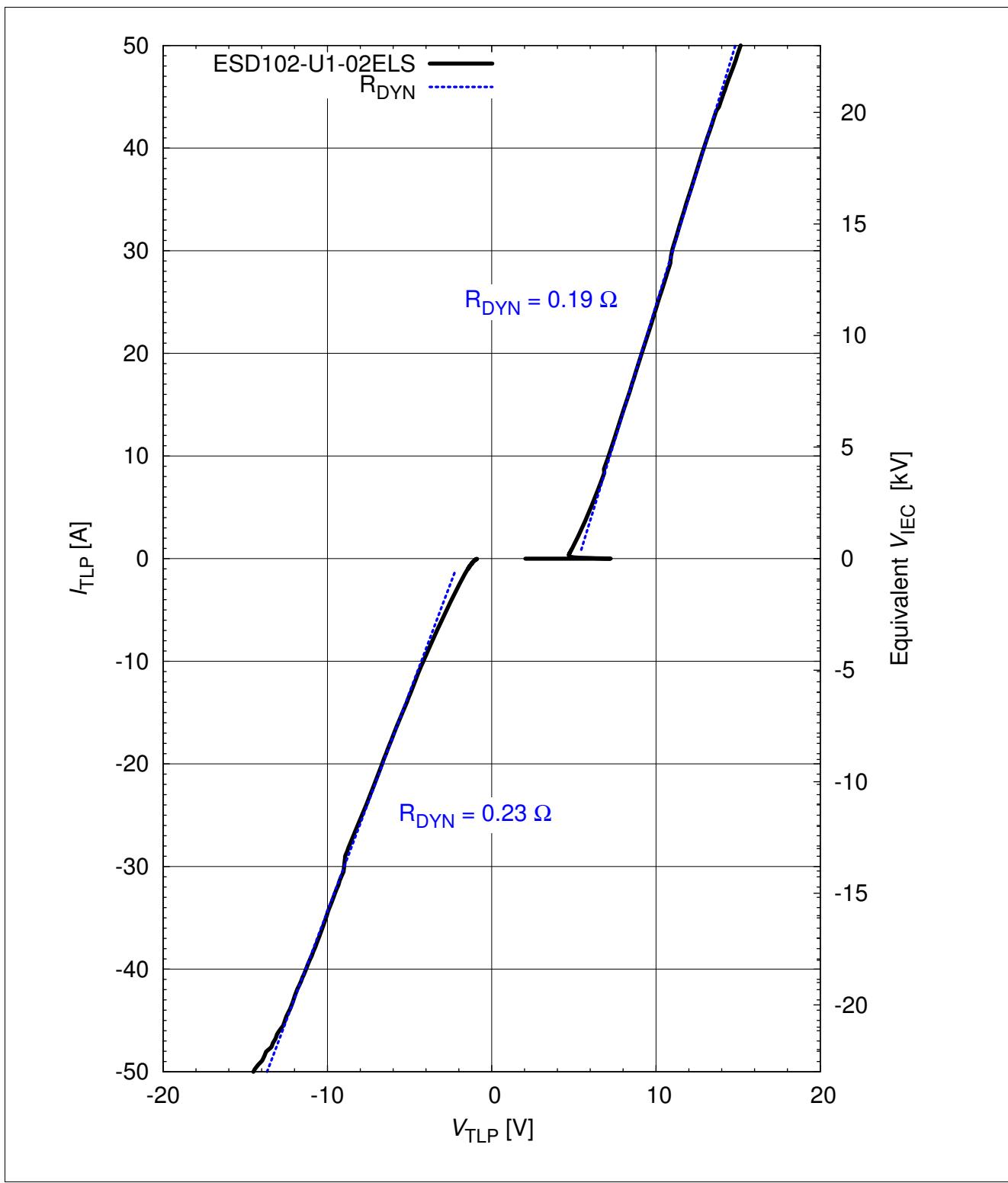
**Characteristics**


**Figure 9** IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV positive pulse from pin 1 to pin 2



**Figure 10** IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV negative pulse from pin 1 to pin 2

## Characteristics



**Figure 11 Clamping voltage  $V_{TLP} = f(I_{TLP})$ , [2]**

Note: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100$  ns,  $t_r = 600$  ps, averaging window:  $t_1 = 30$  ns to  $t_2 = 60$  ns, extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10$  A and  $I_{PP2} = 40$  A. The equivalent stress level  $V_{IEC}$  according IEC 61000-4-2 ( $R = 330 \Omega$ ,  $C = 150$  pF) is calculated at the broad peak of the IEC waveform at  $t = 30$  ns with  $2$  A / kV

## Characteristics

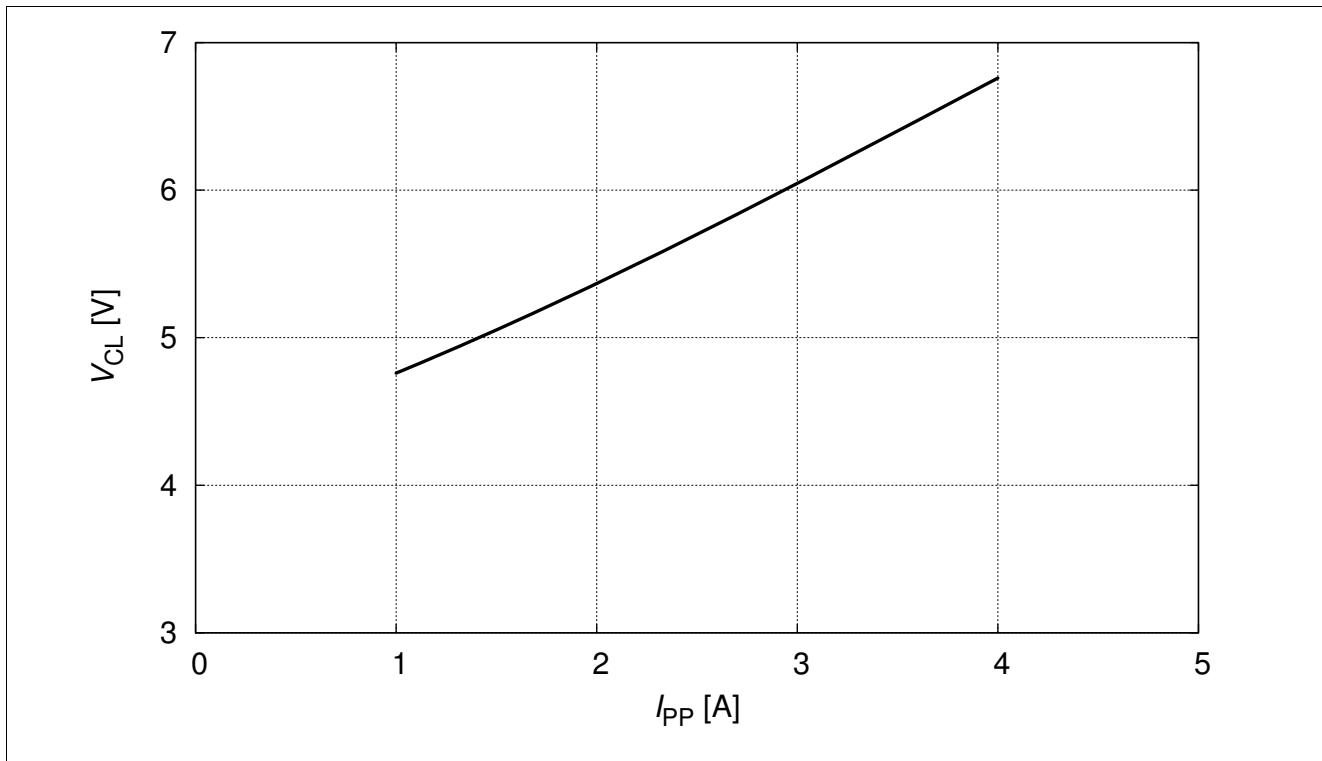


Figure 12 Reverse clamping voltage  $I_{PP} = f(V_{CL})$ , from pin 1 to pin 2 according to IEC61000-4-5 (8/20  $\mu$ s)

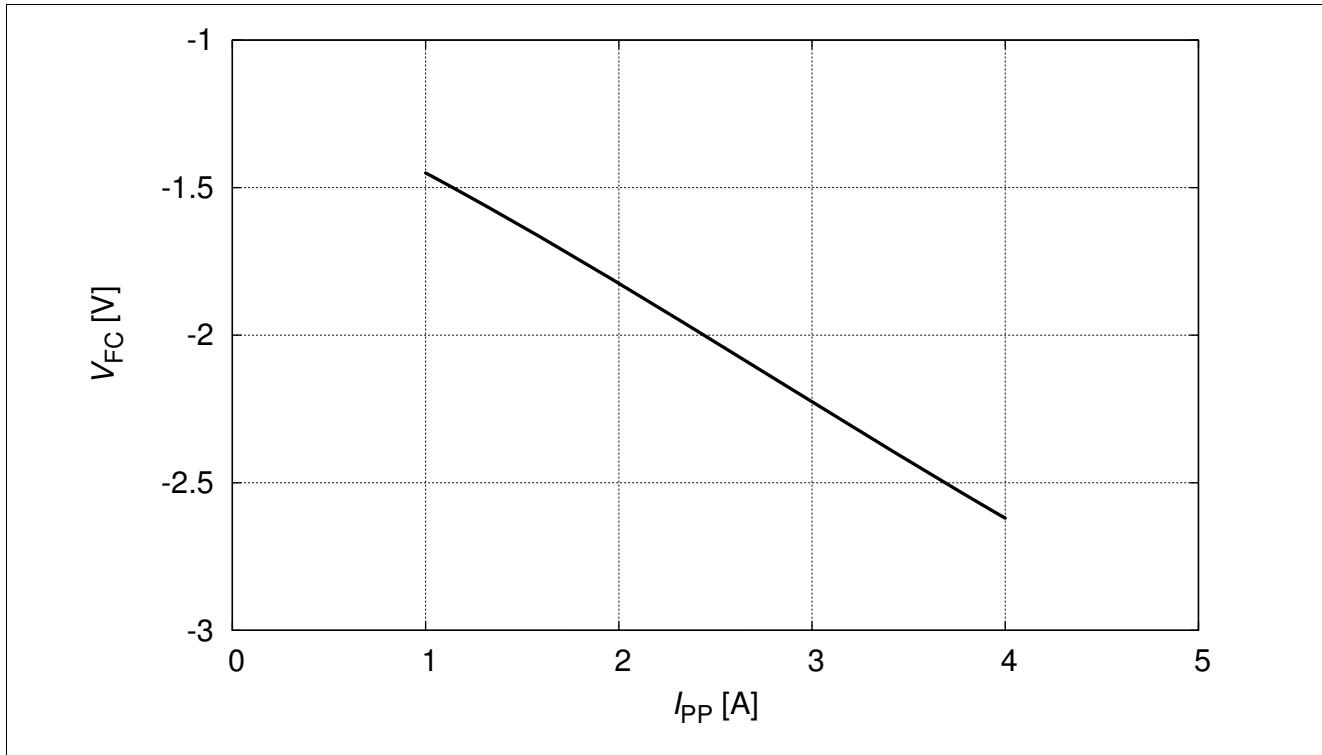


Figure 13 Forward clamping voltage  $I_{PP} = f(V_{FC})$ , from pin 1 to pin 2 according to IEC61000-4-5 (8/20  $\mu$ s)

### 3 Application Information

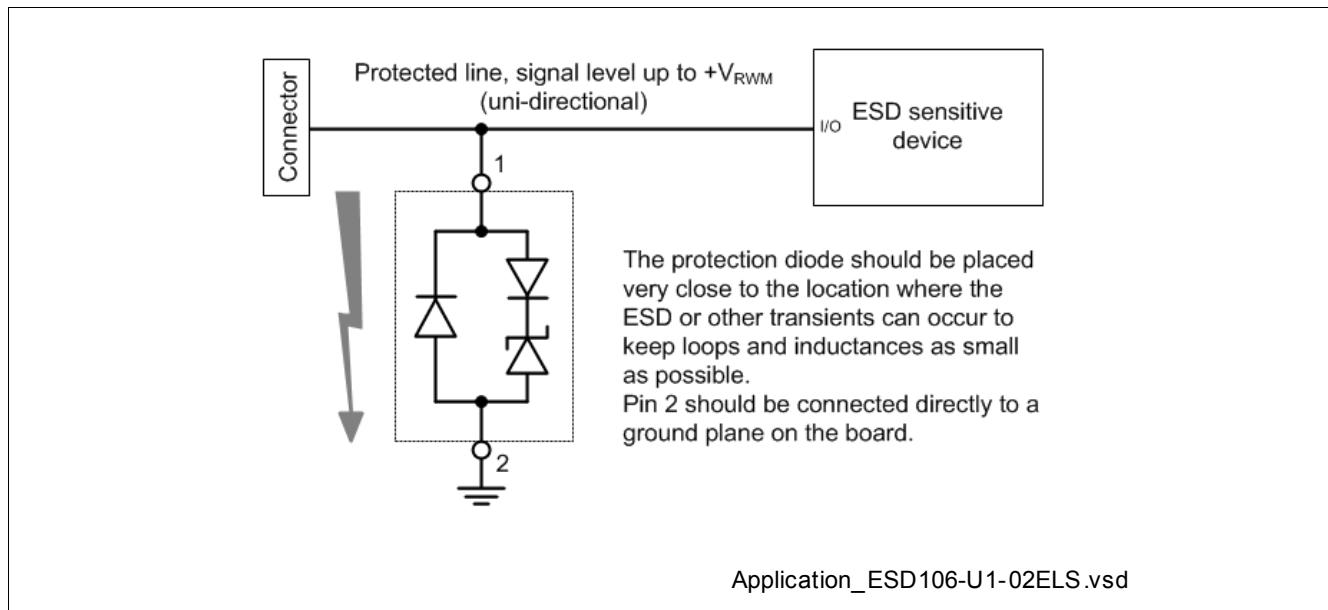
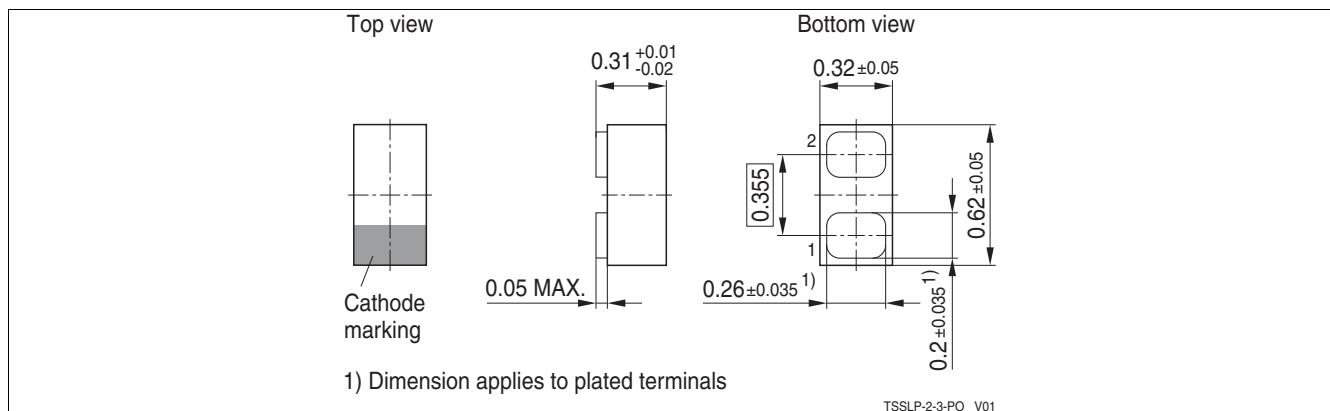


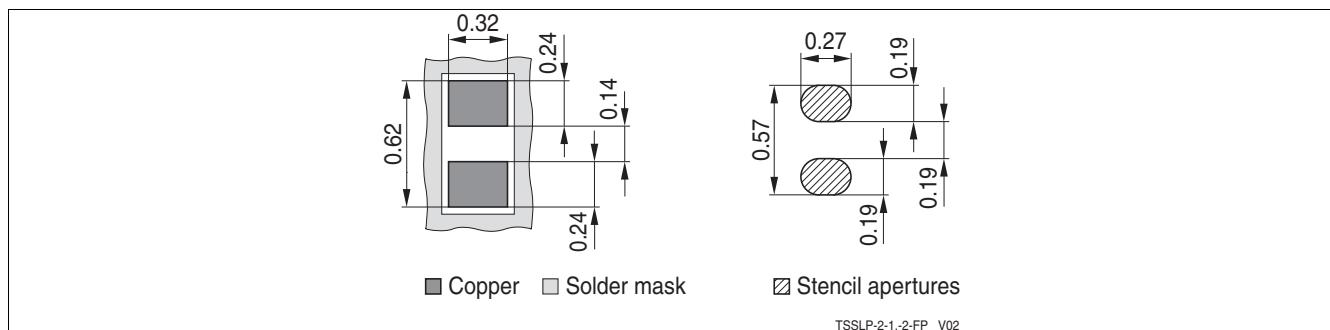
Figure 14 Single line, uni-directional ESD / Transient protection[2]

## 4 Package Information

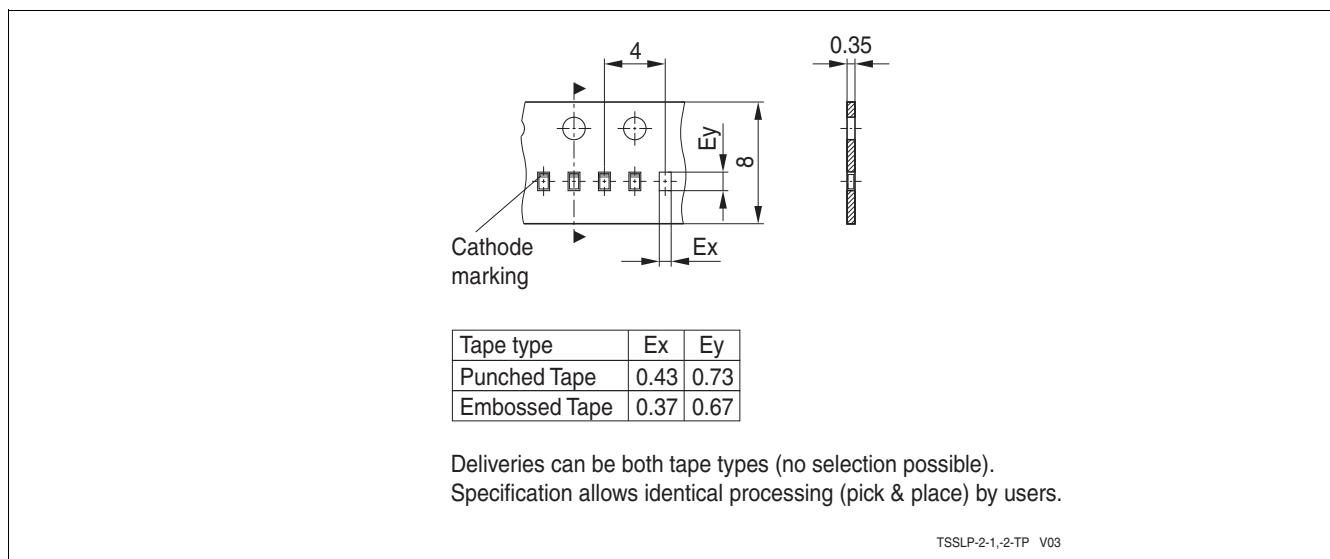
### 4.1 TSSLP-2-3 (mm) [3]



**Figure 15 Package outline for TSSLP-2-3 (dimension in mm)**



**Figure 16 Package footprint for TSSLP-2-3 (dimension in mm)**



**Figure 17 Tape and Reel Information for TSSLP-2-3 (dimension in mm)**

## Package Information

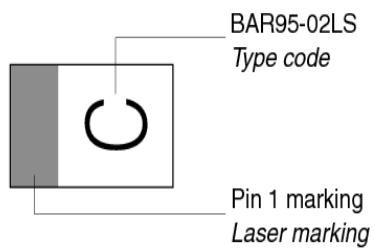


Figure 18 Marking for TSSLP-2-3 (example)

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**References****References**

- [1] On-chip ESD protection for integrated circuits, Albert Z. H. Wang, ISBN:0-7923-7647-1
- [2] Infineon AG - **Application Note AN210:** Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
- [3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

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